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Electronic Package Technology Development

Advanced Package Technologies for High-Performance Systems

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Advanced Package Technologies for High-Performance Systems

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ABSTRACT

Microelectronic packages continue to undergo significant changes to keep pace with the demands of high-performance silicon. From the traditional role of space transformation and mechanical protection, packages have evolved to be a means to cost-effectively manage the increasing demands of power delivery, signal distribution, and heat removal. In the last decade or so, increasing frequency and power levels coupled with lower product costs have been driving new package technologies. Some examples of this are the migration from wirebond to flip chip interconnect and ceramic to organic package substrates.

Recently, architectural changes like the introduction of multicore processors, material changes such as the low-K dielectrics on the silicon, and lead-free second-level interconnects have introduced a new set of challenges that require innovative package technology solutions. As we look forward, increased levels of current, increased power density, and high-bandwidth signaling are expected to create challenges in all disciplines within the package field. In addition to these technical challenges, market forces such as declining computer prices, increased user experience through miniaturized devices, wireless connectivity, and longer battery life would make these challenges even more complex.

In this paper we provide an overview of trends and challenges in the areas of power delivery, signal transfer, thermal management, miniaturization, and wireless package technologies. We also examine some of the potential solutions that are being developed to meet these challenges.

INTRODUCTION

Forty years of improvements in electronic components driven by Moore's Law has made almost all electronic systems relatively high performance when compared to the systems of a few years past. Even many low-cost children's toys today have computing power that exceeds the power of the earliest Personal Computers (PCs). In this paper, however, we limit the scope of our discussion to advanced package technologies used in consumer and business computing devices such as mobile and desktop PCs as well as workstations and servers. Some of the key components in such systems that drive the use of state-of-the-art package technologies are the microprocessors, chipsets, and WLAN components.

The evolution of packages for the desktop PC is shown in Figure 1. In the early 1980s, the 8086 microprocessor chip was housed in a Ceramic Dual In-line Package (CDIP). It used wirebonds to interconnect the silicon chip to the conducting leads on the ceramic package. This 800 mm^2 package had 40 leads placed along its two long sides. With an operating frequency of only a few MHz, fewer than ten percent of the leads were needed to supply power to the chip allowing the majority of the leads to do the useful function of signal transfer in and out of the microprocessors. The primary function of this package was to provide space transformation and environmental protection. By 1994, the Pentium® Pro processor used a 3000mm^2 Ceramic Pin Grid Array (CPGA) package with

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387 pins, a large copper-tungsten heat slug and two chips– the CPU chip and a separate large SRAM cache chip. Over 40% of the pins were dedicated to deliver power to the chips. By the mid-1990s, cost and conductor resistance of the ceramic packages drove another shift in package technology. CPU packages for desktop PCs migrated to Plastic Pin Grid Array (PPGA) that changed the substrate material but continued to use wire bonding for the first-level interconnection. The wire inductance, and the need to have the interconnect pads near the periphery of the chip, significantly degraded the quality of power delivery and limited the chip size shrink. By 1997, advanced processors such as the Pentium® III processor migrated to flip chip BGA and PGA packages. In 2004, the Flip Chip Land Grid Array (FCLGA) package was introduced to eliminate the fragile package pins and enable the second-level interconnect pitch shrink for socketed components.

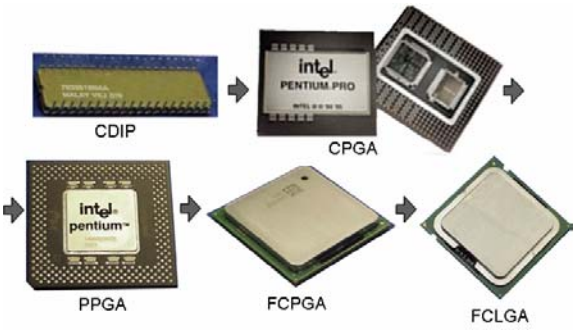

Figure 1: Evolution of Desktop PC package

All of these package changes occurred in an environment of shrinking computer costs (Figure 2). The cost, performance, and form-factor optimizations for different market segments that drove the evolution of package technologies described here also drove many other technologies that are not covered here due to space limitations. Examples of such packages are Single Edge Contact Cartridges (SECC), Organic BGA on socket mountable interposer packages, Tape Carrier Packages (TCP), single- and multi-layer Quad Flat Pack (QFP) packages, etc.

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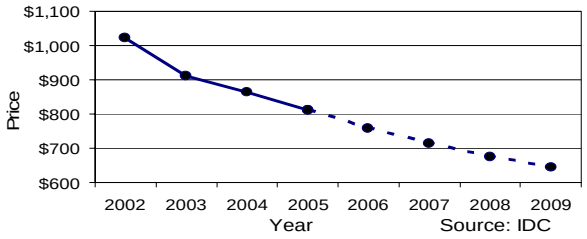

Figure 2: Desktop PC selling price [1]

Package technology continues to evolve to meet changing technical and business challenges. In this paper we explore some of the key issues facing future package technologies and how they are being addressed.

PACKAGE TECHNOLOGY DRIVERS

The traditional microprocessor technology drivers are power delivery, high-speed signal transfer, and heat dissipation. These continue to drive new technologies in advanced packages at every new generation of silicon and product technologies. The recent introduction of multicore CPU architectures has enhanced computing performance without increasing total power. However, lower voltages and some architectural changes drive increases in total current and power density. In addition, for some high-end product segments, higher total power may be necessary to provide significantly higher performance. These require improvements to package power delivery schemes to provide lower noise in power supply.

The increased computing performance requires the signal transfer rate in and out of the processor to increase. In addition, some of the new workloads demand high-bandwidth data transfer between memory and the processor. This leads to higher speed signals on each data line as well as an increase in the number of data lines. However, the relatively slow rate of improvement in motherboard features, such as line width, space and via sizes, makes it difficult to increase the IO count. As a result there has been an emphasis on driving innovation in the area of component-to-component interconnects.

From a thermal management perspective, the benefits of improved performance per watt of multicore technology is somewhat offset by the need for power density increases when one or few of the cores need to consume significantly higher power than the average power per core. With increased current and current densities, the self heating of the package substrate and socket can be as high as many watts even with a large amount of copper in the package and with more than half of the socket pins allocated to power delivery.

In addition to these traditional drivers, there are few new drivers for advanced package technology solutions. One

of the key drivers is the need for lower K dielectrics inside the silicon. These dielectrics, in general, are mechanically weaker requiring the package technologies to manage the stresses on the die.

In order to make the electronic components more environmentally friendly, package materials are being changed to eliminate chemicals like lead and halogen. These changes affect the material properties and processing conditions that need to be managed through proper choice of package technologies.

Platform miniaturization is an important industry trend in mobile platforms. Users are increasingly switching to small computers that are still expected to have robust performance [2]. Overall platform miniaturization requires not only one or two components to be tweaked, but a comprehensive platform approach. As a result, Intel is developing new package designs to take greater advantage of system-level technologies common in the hand-held computing space. For example, in hand-held devices, high density board technology is very common. This type of board technology, often referred to as Type II board technology, removes board routing bottlenecks near the package and thus enables smaller, tighter pitch BGA packages. Such finer pitch packages drive the need for elimination of traditional Plated Through-Holes (PTH) within the package substrates. Furthermore, focusing on the platform solution, Type II board technology allows a reduction in overall platform size by enabling denser component interconnects.

The wireless technologies within the PCs drive a different set of package technologies compared to microprocessor packages. More on each of these is discussed in the following sections.

TECHNOLOGY TRENDS AND CHALLENGES

Power Delivery

As the transistor count and core frequency increase with every new microprocessor generation, current consumption has been growing at an exponential rate. In addition, as the device features get smaller to accommodate the increasing density, the die voltage has been scaling down to satisfy the oxide reliability conditions. This trend dictates a reduction in the impedance of the power delivery network which is proportional to the ratio of the voltage over current. If power levels continue to grow at the same pace, we will soon be faced with a sub-milliohm impedance target over a broad frequency range from DC up to several hundred MHz. Figure 3 plots the impedance target (loadline) as a function of time.

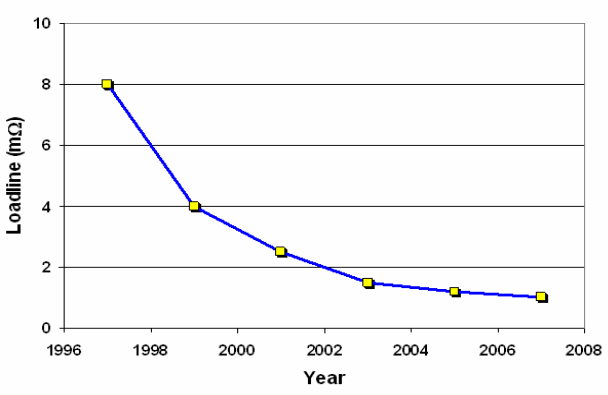

Figure 3: Power-delivery target impedance (loadline) trend

In order to keep up with Moore's Law, the number of transistors on a chip approximately doubles every generation resulting in improved performance. In order to double the device density, key silicon feature sizes are scaled by a factor of 0.7 with each new technology. However, there is a fundamental limit to how fine the features can be. Today's transistor gate oxide layers are literally only a few atoms in thickness. Even good insulators like the gate oxide layers will start leaking current at these dimensions. The leakage power levels in today's microprocessors are an appreciable percentage of the overall power budget. The leakage power issue is typically addressed through a combination of process-level and architectural fixes. Process-level fixes like the use of thicker high k gate dielectrics are usually transparent to microelectronic packages. However, architectural changes like the use of sleep transistors or the switch to multicore processors do have a significant impact on the package solution.

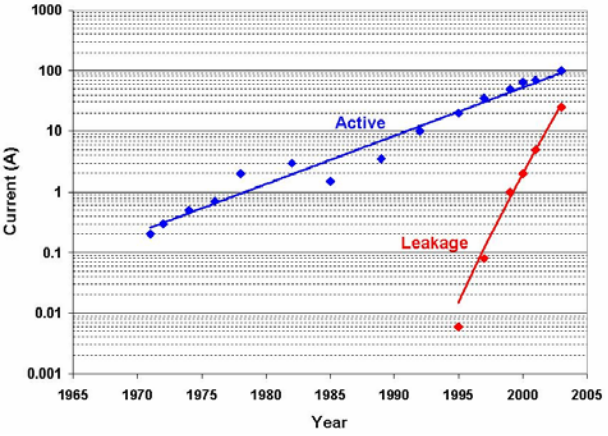

Figure 4: Growth rate of leakage compared to active power

Until recently, the traditional approach to microprocessor design involved shrinking the device features to enable faster switching and higher core frequency. Unfortunately, this tends to increase leakage power, which degrades the processor performance-to-power consumption ratio. A better alternative is to de-emphasize frequency and get better performance by alternate means. De-emphasizing frequency allows the designer to limit the threshold voltage scaling, which keeps the leakage power in check. Performance improvement can still be realized by adding additional cores. For example, by adding an additional core and keeping the frequency flat, it will be possible to get a much higher performance-to-power ratio. One issue with adding additional cores is the impact on the package decoupling solution. Intel processors have traditionally used package land-side capacitors in the socket cavity directly under the core of the processor. However, with multicore processors, some of these cores may overlap the package pin-field resulting in a high-inductance path to the package capacitors.

High-Speed Signaling

With the increase in the processing power of the CPU, the CPU-MCH (Memory Controller Hub), MCH-memory and/or CPU-memory interconnect links need to have exponentially higher bandwidth in order to fully utilize this computing power. Multiple high-resolution media streams in and out in real time also drive high-bandwidth requirements on the graphics side. Figure 5 shows Intel's CPU core frequency, traditional bandwidth, and "scaled" multicore bandwidth requirements. Well-known means to achieve increased bandwidth include increased data rate, increased IO count, and moving the chips closer to each other. High-bandwidth data transfer would drive the CPU Front Side Bus (FSB) to a series differential bus for its higher data rate and flexibility in scaling bus width. The package and socket technology as well as the designs need special attention to take full advantage of the technology.

Enabling a high data rate brings big challenges to package and socket analysis, characterization, and technology development. It is well known that at low frequencies, the package and socket can be treated as R, L, and C elements because their electrical length is much shorter than a wavelength. When a signal moves faster, the package and socket behave as long interconnects and therefore a full wave analysis is needed. For example, we need to treat package horizontal routing as transmission line and via, PTH and socket pins as arbitrary shaped 3D objects for full wave characterizations and designs. Manufacturing tolerance, which can be ignored at low frequency data rates, becomes important at high frequencies and therefore special attention must be paid to this. Moreover, high density and small form-factor requirements push package-level transmission lines to a very small cross section and the insertion loss becomes a dominant part of the whole system loss budget.

High loss package transmission lines and long motherboard transmission lines at high frequencies eventually restrict high data rates. In these cases, it might be necessary to move chips closer together. For instance, moving the Random Access Memory (RAM) chips closer to the CPU benefits RAM performance, such as fully buffered DIMM (FBD) technology. However, the data rate or performance improvement resulting from this move may still not meet the bandwidth requirement, which is increasing exponentially. Thus, more IO interfaces or IO counts are necessary to leverage the flexibility provided by the series signal interface. With the assumption of low-cost infrastructure, increasing the IO count leads primarily to a shrinking interconnect conductor cross section and signal-to-signal pitch for package horizontal transmission lines, micro-vias, PTHs, and socket pin or BGA balls. While via and PTH geometry and cross-section shrinks have only a minimal impact on signal integrity due to their short length, transmission lines and high socket pin counts impact signal performance significantly. Nevertheless, there is a net bandwidth benefit in increasing the number of IOs. However, limitations on the number of second-level interconnects, i.e., socket pins or BGA balls due to cost and size, can cause bottlenecks in the overall system bandwidth by limiting IO counts.

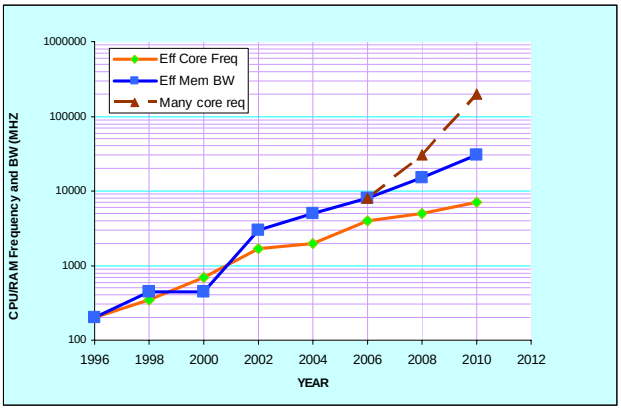

Figure 5: CPU core frequency and bandwidth trend

Thermal Management

We discussed earlier that even at constant power, the power density and electrical current is expected to increase. As current levels continue to rise, Joule heating, i.e., heat generated when current passes through a resistor, along the power delivery path becomes significant. Since it is not uncommon for today's high-end microprocessor to draw currents in excess of 100A, even a resistance of 0.5mΩ along the path will result in a power dissipation of 5W. Thus it will be increasingly critical to do the thermal

management of the on-chip hotspots as well as the package and socket Joule heating.

Power Density

Thermal designers need to account for thermal non-uniformity (typically referred to as hotspots, where power densities of 300+W/cm^2 are possible) caused by non-uniform distribution of power on the die. To help quantify the non-uniform power effects, a Density Factor (DF) that is independent of the power profile on the die has been proposed [3]. The DF is simply the ratio of the actual package thermal resistance at the hottest spot to the die-area-normalized uniform power resistance or thermal impedance, and has the units of inverse area (A^{-1}). DF can be used to quantify the impact of non-uniform die heating on thermal management. Equation (1) shows the relationship of package junction-to-case thermal resistance (ψjc) to the package thermal interface material technology (Rjc).

$$\psi jc = Rjc * DF \quad (1)$$

It can be seen that for the same package thermal interface material technology being used (i.e., the same Rjc value), the power maps with a higher DF will result in a higher package thermal resistance, which in turn requires more advanced cooling solutions. Figure 6 shows the increasing trend of DF for desktop microprocessors due to the increasing local power density at the hotspots.

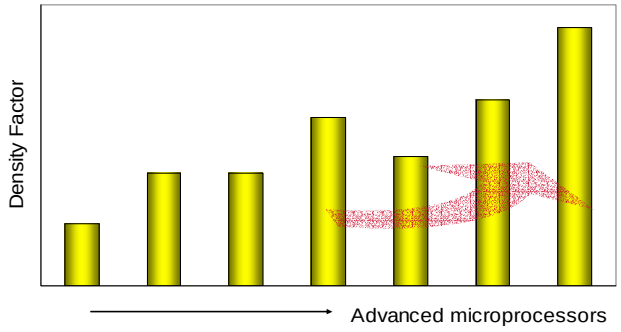

Figure 6: Density Factor trend for typical desktop microprocessors

Joule Heating

Higher current combined with the need to reduce the package size, i.e., thinner and narrower conductors and/or finer pitch power delivery interconnects, would lead to a high amount of heat generated within the package and socket. This would require thermal management of the entire interconnect which includes the flip chip joints, the substrate, the socket and the solder balls. Figure 7 shows an example of a temperature map of the metal contacts in the socket due to Joule heating. The lighter color here indicates higher temperatures.

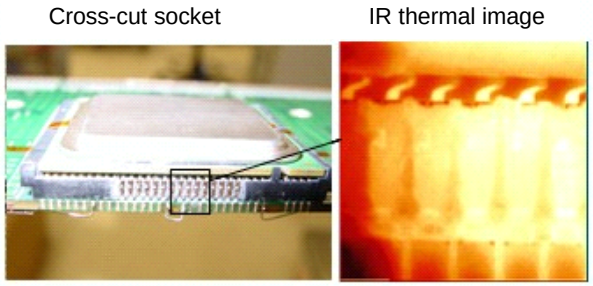

Figure 7: Example of Joule heating of socket contact pins

One key area of challenge is the increasing temperature of the flip-chip die bumps. As the electrical current through the flip-chip die bumps and the substrate traces increases, Joule heating increases the bump temperature (Tb) when compared to the transistor junction temperature (Tj) as shown in Figure 8. Without proper attention to package design, the bump temperature could be significantly higher than the Tj causing bump electro-migration problems. The socket and substrate temperatures can also rise due to Joule heating.

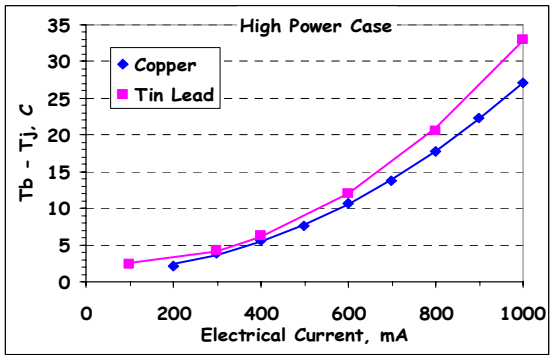

Figure 8: Temperature difference between die bump (Tb) and die (Tj) for two different bump materials

Die Stacking

Stacked die packages are a recent trend for memory chips for handheld devices and possibly could be used in conjunction with CPU or chipsets in the future (Figure 9). The thermal challenge of stacked die packages is largely due to higher power dissipation and higher thermal resistance between dies.

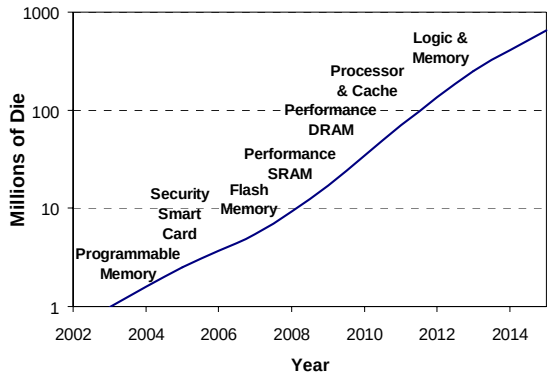

Figure 9: 3D Die stacking trend (source: Prismark)

Miniaturization

Mobile computing has been one of the world's fastest growing PC market segments [1], and Intel is delivering many products to meet the needs of mobile computing. For example, to enable wireless communications on mobile computing platforms, Intel® Centrino® mobile technology was developed. Moving forward, miniaturization with increased functionality continues to be an important trend in mobile computing. An example of the miniaturization trend is also seen in the ever improving functionality of mobile handsets. Over the last five or so years, 2D games, and now more demanding 3D games, have become available in these devices. Also, within the last year or so, handset and content providers have teamed up to bring video content to the newest handsets. As more and more functionality is driven into smaller platforms, there will be an ever increasing pressure on component and platform-level solutions to provide smaller packages and denser interconnect solutions.

Packages for Wireless Devices

Traditionally, wireless communication devices as illustrated in the block diagram of Figure 10 have consisted of a mixture of several active devices from different semiconductor technologies such as silicon CMOS, silicon BiCMOS, GaAs, and SiGe, all of which are mounted on a PCB substrate and supported by numerous passive components. Each die is typically packaged in a Quad Flat No-lead (QFN) package using low-cost wirebond technology.

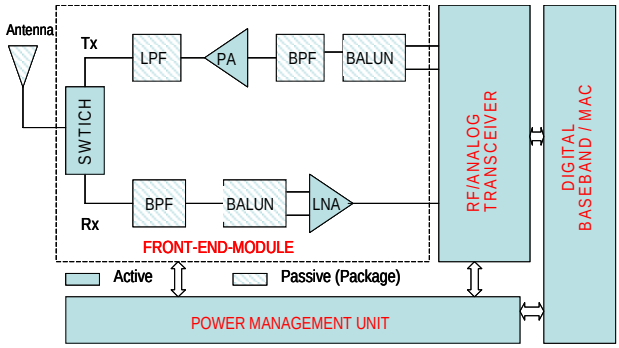

Figure 10: Block diagram illustration of a single band wireless communication device

With the improved maturity of CMOS technologies, the bulk of wireless communication devices is expected to evolve in the short term to a two-chip solution, where one chip is dedicated to RF/analog (radio) and the other chip is dedicated to the digital (baseband/MAC). Over the long term, however, it is expected that the maturity of CMOS technology and improved signal isolation techniques will enable a single-chip solution, where baseband, radio, and even the power amplifier, typically found on the front-end-module, are all integrated on the same silicon substrate. The increased level of integration is expected to require larger package pin counts and possibly larger package sizes, as illustrated in Figure 11. The evolution of wireless devices to multimode, multiband devices that can operate worldwide and provide functionalities such as GSM, PCS, UWB, Wi-Fi*, WiMax, and GPS requires that future devices be implemented as multiband radios. As the frequency of operation increases, improvement in channel capacity and recovery of signal attenuation associated with interconnect losses require that multiple inputs and multiple output (MIMO) radio architectures be adopted. The addition of each frequency band for multiband radios or an additional transmission path for MIMO has a direct implication on the number of IOs needed by the first-level package. As the total pin count exceeds 70, the traditional single-row QFN would face significant challenges driven by the leadframe metal pitch constraints and the required RF signal isolation between adjacent signal lines.

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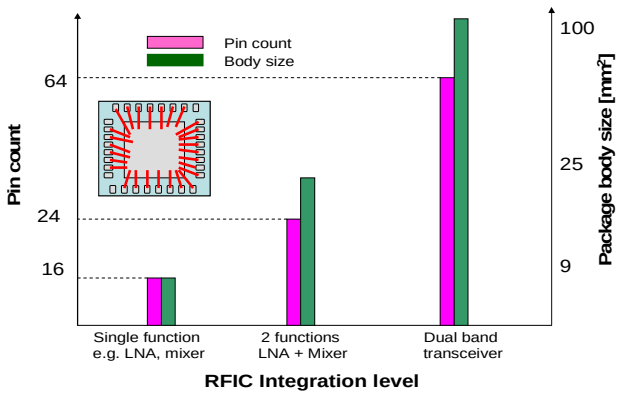

Figure 11: Package pin count and body size requirements for integrated wireless solutions

The increased functionality (music, video, gaming, etc.) integration with each handheld product generation adds to the complexity of the baseband and power management units, which in turn requires more passive components (especially resistors and capacitors) for baseband power supply and management. For example, the number of passive components in a typical cellular phone has more than tripled over the last few years. This increase in passive counts leads to increased assembly costs and reliability issues.

The second level of wireless package is at the module level and includes critical building blocks such as filters, diplexers, baluns, and matching networks found in the RF Front-End Module (FEM). As illustrated in Figure 10, for each frequency band, complete transmission and receive paths are needed. For both multiband and MIMO radios, this implies a significant increase in the overall real estate of the FEM and the wireless device in general. Despite the increase in the number of frequency bands and the implementation of MIMO radios, the size of the package at the module level is expected to continue to decrease as a result of the requirements of portability and power consumption. This would require, for example, that stringent isolation techniques be used at the package level for proper signal isolation between the different transmission paths of the MIMO radios. At the same time, innovative substrate solutions have to be developed to deliver small form-factor filters, diplexers, baluns, and matching networks.

POTENTIAL SOLUTIONS

Power Delivery

Meeting sub-milliohm power delivery impedance targets and containing leakage power are two major challenges that influence the design of the power delivery solution in today's microprocessors. Since the spectral content of the current drawn by the processor is fairly broad-band, it is important to have a low impedance path from the power supply to the microprocessor across a wide range of frequencies from DC up to several hundred MHz. In order to manage the high-frequency noise, Intel microprocessors have been steadily migrating to better performance package capacitors. Starting with the first Pentium® processor and up until the Pentium III processor, 2-terminal capacitors were used for package decoupling. Starting with the Pentium® 4 processor, package decoupling needs were addressed using Inter-Digitated Capacitors (IDC). These capacitors have eight alternating power and ground terminals that help reduce the effective inductance, thereby reducing the high-frequency noise seen by the processor. As the power supply demand goes up, even the performance afforded by the IDC capacitor will become inadequate. There are more advanced capacitors such as array capacitors that are currently being investigated as a potential decoupling option for future processors. Array capacitors tend to have a large number of power and ground terminals that make their effective inductance vanishingly small. Figure 12 shows a picture of the different capacitors that are discussed here.

Figure 12: Evolution of package capacitors

As the improvement in capacitor technology drives down the effective inductance of the capacitors, the inductance of the package interconnect becomes the performance bottleneck. This is especially true in the case of multicore processors with one or more cores overlapping the package pin-field. In such cases, the best option would be to use embedded capacitors placed inside the package directly under the cores.

The advanced capacitor solutions limit the high-frequency noise but have little impact on the low-frequency noise seen by the microprocessor. One way to limit the low-frequency noise is to reduce the resistance in the path from the VR to the die. The DC resistance is typically managed by adding more power and ground pins and increasing the copper thickness in the package power and ground layers. Figure 13 shows a picture of the different types of sockets that have been used over the past few years. As shown in the pictures, the number of pins in the

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socket has gone up each time we transition to a new socket. At the same time the socket pin pitch has been scaling down, which allows us to increase the pin count without driving up the package body size. Another option to minimize the resistance in the path involves moving the Voltage Regulator (VR) closer to the die. One such topology moves the VR components from the motherboard to a custom VR board that is sandwiched between the package and the heatsink. The power flows from the VR board to the package through an LGA connector. Apart from moving the VR closer to the die, this concept also frees up the P/G pins in the socket which can now be used to address signaling needs. While moving the VR closer to the die provides incremental performance benefits, the ultimate power delivery solution would be to integrate the VR components on the load die or to attach the VR die directly on the top or bottom of the load die.

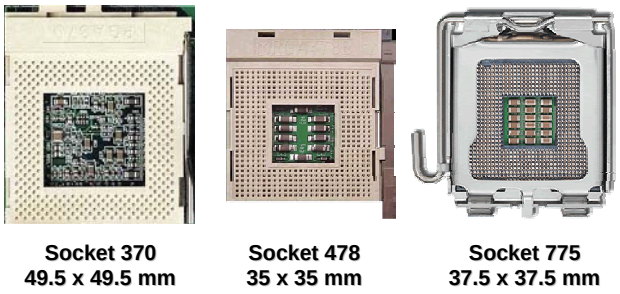


Figure 13: Evolution of socket technology

High-Speed Signaling

Increasing the data rate is generally the first choice to enable a high-bandwidth system. Typically, two approaches are taken to enhance data speed, namely, loss management and impedance control. While package transmission line loss is mainly due to conductor loss, the copper conductors being used in the organic packages today already provide excellent conductivity. There is not much room for further optimization due to physical limitations. Focus is then shifted to impedance control. Although signal integrity engineers already noticed that packages typically behave as a capacitor such that their impedance is lower than the overall interconnect, and designers already decreased the system impedance target from 100ohm to 90ohm and are now targeting 85ohm, specific package treatments are still necessary to achieve high bandwidth. A key optimization approach is to reduce signal path capacitance so that the "characteristic" impedance can be moved up to match system impedance, resulting in a smaller return loss and a higher insertion loss. Figure 14 shows FCLGA package insertion loss with reduced capacitance between bottom layer pads to the upper layer ground plane. Other approaches to reduce capacitance include smaller socket pad size or locating a spiral inductor to balance capacitive effects.

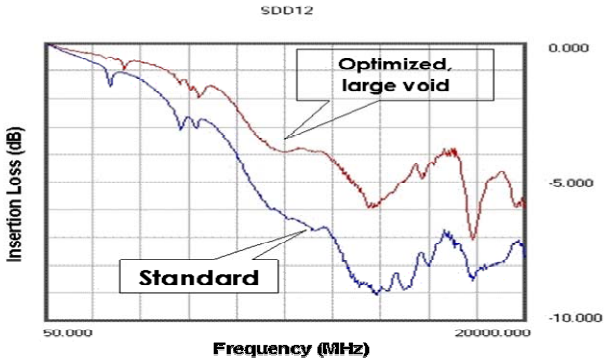


Figure 14: Optimization of package interconnect design for high-speed signaling

Bandwidth increases from optimization of current interconnect paths or from positioning CPU, chipset and RAM packages closer may not be enough to meet the demands of high-performance computing and multi-media applications. Increasing the IO count also has issues with second-level interconnect density, package sizes, and cost. As a result, revolutionary solutions are needed. Here we show two approaches: one uses an MCP configuration, i.e., putting CPU and RAM side by side (2D configuration) on a single package, and the other uses a 3D stacking approach, i.e., mounting the CPU on a RAM that has through silicon vias in the RAM. Figure 15 shows the basic idea of these two approaches. 2D MCP can provide a few hundred GB/s bandwidth based on projected RAM performance around 2010. However, in order to achieve an order of magnitude higher bandwidth, 3D stacking of the chips would be needed. The 3D stacking not only provides very high interconnect density, but also delivers bandwidth efficiency through higher data rate and improved power consumption.

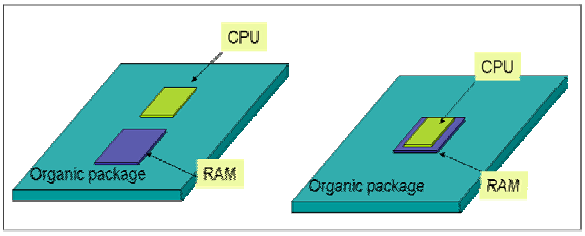


Figure 15: MCP and 3D die stacking approaches for high-bandwidth system

Thermal Management

Quite a few technologies are under evaluation by industrial and academic researchers. One area of research is to enhance convection cooling by improving the heat transfer coefficient through extended heat sink surfaces and high airflow fans with the built-in feature for acoustic

noise cancellation. Attention has also been paid to the development of heat spreader material such as carbon fiber, graphite, thermal-conductive composites, vapor chambers, heat pipes, and nano-materials. The researchers are aggressively seeking solutions beyond air cooling. For example, a closed-loop liquid cooling system, as shown in Figure 16, is under development. This system implements cold plates or micro-channels with either single-phase or two-phase liquid cooling. In addition, refrigeration to achieve "negative" thermal resistance is being developed with the focus on reducing the size and cost of the compressor and the heat exchanger. Recently, researchers also have investigated solid-state refrigeration (or thermoelectric coolers) for "hotspot" cooling of devices with highly non-uniform power dissipation (Figure 17) or full-chip cooling in conjunction with vapor chamber heat sinks. This type of technology can actively cool the electronic device temperature with no moving parts and potentially provide "negative" thermal resistance similar to traditional refrigeration. Emerging nano-materials hold promise of providing highly conductive Thermal Interface Materials (nano-TIMs) and reducing interconnect Joule heating.

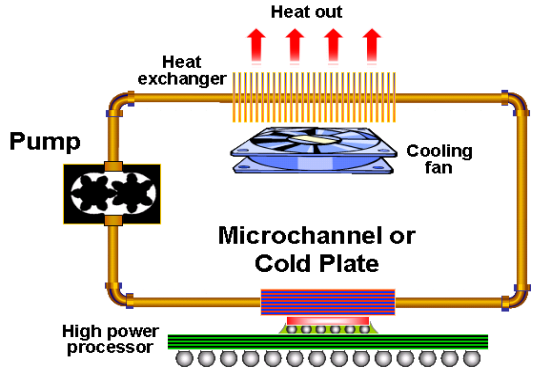


Figure 16: A schematic for a typical closed-loop liquid cooling system

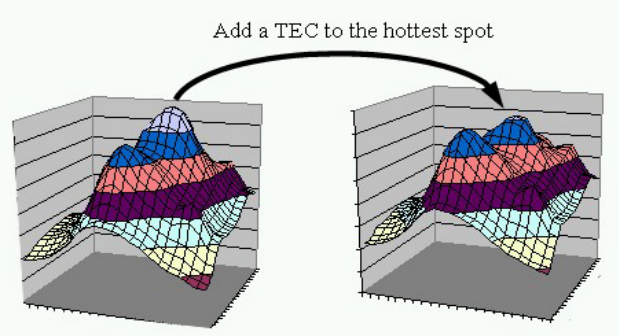


Figure 17: Example of hotspot suppression by applying a TEC to the hottest spot

The Joule heating of the interconnects on the package and socket can be effectively managed through careful design and analysis. This involves minimizing current concentration and spreading heat away through design and material choices.

Miniaturization

While it can be a challenge to deliver greater functionality in dramatically smaller packages, mobile and small form-factor platforms also offer opportunities for package designers. One example is Type II board technology (Figures 18, 19). Such a board employs buried vias and "micro vias" (µvias) as well as smaller feature sizes. In contrast, mobile PC boards may often have only PTHs and larger feature sizes. A typical desktop board often has even larger PTHs and feature sizes and it has fewer layers than mobile boards. The features of the Type II board technology help in breaking signals out of the package and in delivering power to the package. Figure 20 illustrates this point. The first example used mobile board features. Here the package ball pitch reduction is limited by the need to fit board PTHs in between the BGA pads. Larger board feature sizes, such as signal trace width, further impede package miniaturization. This can result in a package BGA pitch reduction limit of around 0.8mm. On the other hand, Type II board features can result in a package breakout similar to that shown in the second example of Figure 20. Here the package BGA pitch has been reduced to around 0.6mm. This results in significant increase in BGA density and a reduction in package size.

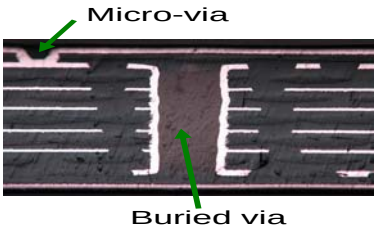


Figure 18: Typical Type II board stackup

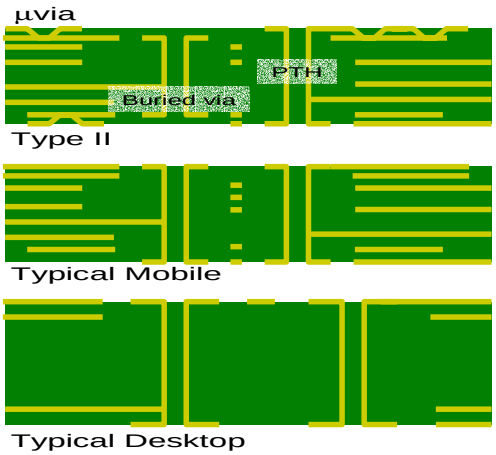


Figure 19: Schematic representation of typical board features from desktop

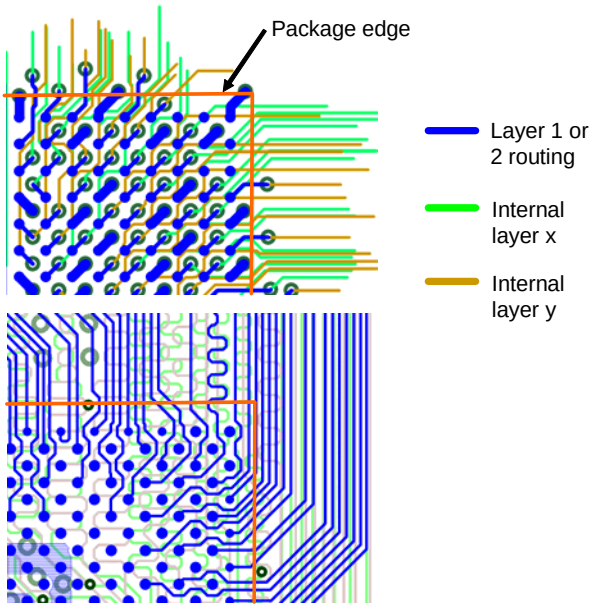


Figure 20: Illustration of routing fan-out differences between typical mobile (top) & Type II (bottom) board

As board routing capabilities increase, the large size and pitch of the package PTHs can constrain the BGA ball pitch shrink. The solution is to use smaller size PTHs with thinner core package substrates or to eliminate PTHs through the use of coreless packages. Figure 21 illustrates potential density improvements for typical thin core and coreless cases. Similarly, innovations in robust power delivery decoupling solutions are being researched. This includes eliminating the decoupling capacitors or minimizing their size and quantity, or cost-effectively embedding the capacitors in the substrate.

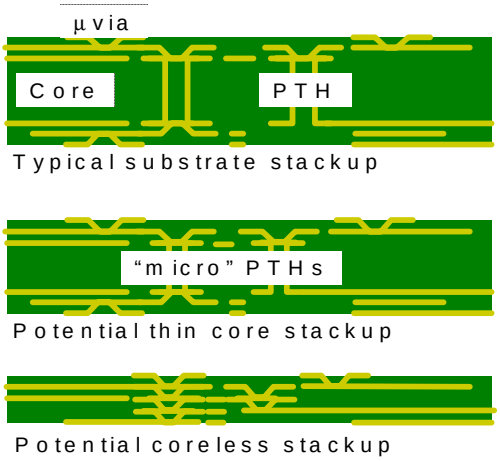


Figure 21: Schematic of typical, thin core, and coreless package stackups

Wireless Packages

High-pin Count Package Solutions

The problem of limited pin counts associated with QFN packages for highly integrated wireless systems is addressed by using dual-row QFN packages [4] instead of the traditional QFN packages in which two rows of surface mount pads are placed at the periphery of the package. Both rows can then be connected to the die using wirebonds. This technology, as illustrated in Figure 22, can provide about 150 IOs for a package with a body size of 12mm x 12mm, which is sufficient for a dual-band MIMO GSM or WLAN radio.

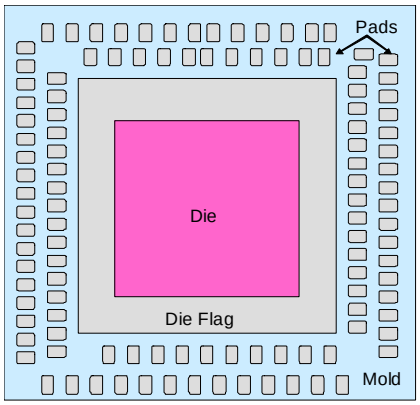
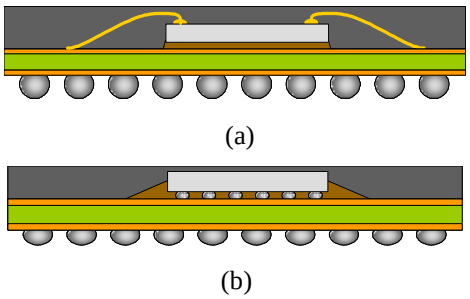


Figure 22: Dual-row QFN for wireless chip

As the RF/analog and digital ICs are combined on a single silicon die and the number of IOs goes beyond 170, the package options available are traditional MMAP (Figure 23), carrier tape-based leadframe packages, or a simple extension of QFN technology.



(a)

(b)

Figure 23: MMAP package technologies for high pin-count wireless chips in (a) wirebond and (b) flip-chip configurations

Embedded Passives for Baseband Power Management and Miniaturized Front-end Modules

At the board level, most passives (mainly resistors and capacitors) used for the baseband power supply are experiencing a gradual size reduction from today's standard 0603 to smaller 0201 to meet the stringent form-factor requirements. In parallel, embedded passives technologies, where all resistors and capacitors are fabricated as part of the package substrate, are gaining more importance, not only because this technology reduces space, but also because it has the opportunity to enhance product reliability by reducing or eliminating the solder joints. Figure 24 shows a size comparison between typical surface mount and embedded capacitors. Due to the wide capacitance range and tight tolerance demands on these passives, significant innovation is required in integrating the high-K dielectrics to fully utilize the benefits of embedded passives technology.

RF Front-end Module Solutions

In the RF FEM, the development of low-temperature co-fired ceramic and multilayer organic substrates to include high-performance inductors and capacitors has paved the way to integrate filters, diplexers, and LC-based matching networks with much smaller form factors. At the same time GaAs and silicon-based integrated passives have shown good electrical performance for RF FEM applications. The extremely good quality factor of package-embedded inductors will enable future WiFi/WiMax radios to have FEM, where all filtering functions are based exclusively on capacitors and inductors embedded in the package substrate, leaving the surface for the active dies. A detailed discussion of embedded passives for miniaturized front-end-modules can be found in "Future Package Solutions for Wireless Communication Systems" in this issue of the *Intel Technology Journal* [5].

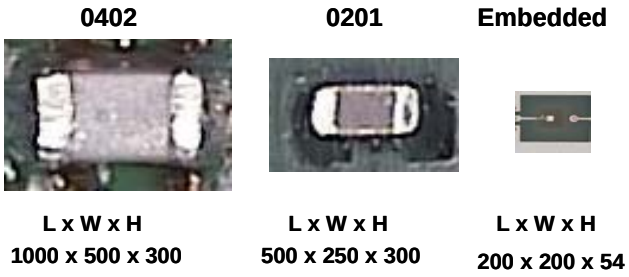


Figure 24: SMT and embedded capacitor size comparison. All dimension (W,L,H) are in µm

SUMMARY

An overview of the key challenges and potential solutions was presented for advanced microelectronic packages in the computing systems commonly used by today's consumers and businesses. Higher performance levels of the key ICs in these systems demand reduced noise in the power supply path from the VR to the transistors on the silicon. Similarly, higher signal transfer bandwidths between different components are needed to feed the data to the high-performance computing engines. Package technology has cost-effectively come up with solutions without significant system architectural changes. In many cases, the VR and the memory components are brought electrically closer to the load die such as the microprocessor, but are still kept off the load die package. The tricks used to achieve these are providing diminishing returns. The trend to reduce the electrical distance to the VR and the RAM would eventually lead to these components being physically brought onto the package in the form of a multi-chip package solution. This will lead to physical space contentions on the small package. Such multi-chip packages are expected to solve these issues for a few more generations but will add complexity to package technology. A further drive to bring the components closer would require the different dies to be vertically stacked and interconnected through features like through-silicon vias. This will create significant challenges not only to many aspects of package technology but also to silicon technology, product architecture, and IC design technology.

Handheld market segments offer an intriguing motivation and opportunity for IC package and platform miniaturization. Platform technologies more common in this segment, e.g., Type II board technology, enables sub-0.8mm BGA pitch for microprocessors and chipsets. Advances in package technology such as thin-core and coreless substrates may push the miniaturization envelope even further by reducing or eliminating the package PTH bottleneck. At this point, a blurring of the traditional role between package and board may emerge allowing for even smaller platform form factors.

The form factor and cost demands of the wireless products drive the need to manage the passive components within the package effectively.

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